DDR2 Register Memory Module

AETx61PDxx-30DxxxX

512MB, 1GB, 2GB, 4GB

This Data Sheet describes AENEON DDR2 Registered DIMM on 240-pin modules with parity bit for address and control bus and its main characteristics.

Key features

- Registered DDR2 memory modules with address parity bit
- Available in single pack of densities 512MB/1GB/2GB/4GB
- Standard Industry Standard pin configuration
- Fully RoHS compliant

TABLE 1
Ordering Information

Product Type[1)]	Module Density	Organization	Rank Organization	Module Speed	No of Comp	Module Size(mm)
AET661PD00-30DB19X	512MB	64M x 72	1Rx8	PC2-5300-555	9	133.5 x 30 x 8.2
AET761PD00-30DB19X	1GB	128M x 72	1Rx4		18	
AET761PD14-30DB29X	1GB	128M x 72	1Rx4		18	
AET861PD00-30DB19X	2GB	256M x 72	2Rx4		36	
AET861PD24-30DB29X	2GB	256M x 72	2Rx4		36	
AET861PD14-30DC20X	2GB	256M x 72	1Rx4		18	
AET961PD24-30DC20X	4GB	512M x 72	2Rx4		36	
AET961PD00-30DB10X	4GB	512M x 72	2Rx4		18 DDP	

1) Full Product Type / Sales Description

TABLE 2
Speed Grade Definition

Speed Grade		PC2	-5300			
CAS-RCD-RP latencies			5–5–5			
Parameter		**Symbol**	**Min.**	**Max.**	**Unit**	**Note**
Clock Period	@ CL = 3	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3	8	ns	1)2)3)4)

Speed Grade	PC2	–5300			
CAS-RCD-RP latencies		5–5–5			
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Note**
Row Active Time	t_{RAS}	45	70k	ns	1)2)3)4)5)6)
Row Active Time	t_{RAS}	40	70k	ns	1)2)3)4)5)7)
Row Cycle Time	t_{RC}	60	—	ns	1)2)3)4)
Row Cycle Time	t_{RC}	55	–	ns	1)2)3)4)
RAS-CAS-Delay	t_{RCD}	15	—	ns	1)2)3)4)
Row Precharge Time	t_{RP}	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode.
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ}
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.
6) Products released after 2007-08-01 can support $t_{RAS.MIN}$ = 40 ns for all DDR2 speed sort.
7) For products released after 2007-08-01.

TABLE 3
DC Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.5 × V_{DDQ}	0.51 × V_{DDQ}	V	2)
SPD Supply Voltage	V_{DDSPD}	1.7	—	3.6	V	
DC Input Logic High	$V_{IH(DC)}$	V_{REF} + 0.125	—	V_{DDQ} + 0.3	V	
DC Input Logic Low	$V_{IL\ (DC)}$	– 0.30	—	V_{REF} – 0.125	V	
In / Output Leakage Current	I_L	– 5	—	5	µA	3)

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}
2) Peak to peak AC noise on V_{REF} may not exceed ± 2% V_{REF} (DC). V_{REF} is also expected to track noise in V_{DDQ}.
3) Input voltage for any connector pin under test of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V; all other pins at 0 V. Current is per pin

Attention:Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 4
Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–1.0	+2.3	V	1)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.5	+2.3	V	
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	–0.5	+2.3	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.5	+2.3	V	

1) When V_{DD} and V_{DDQ} and V_{DDL} are less than 500 mV; V_{REF} may be equal to or less than 300 mV.

TABLE 5
Environmental Requirements

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Operating temperature (ambient)	T_{OPR}	–	–	°C	1)
Operating temperature (ambient)	T_{OPR}	0	+55	°C	2)
Operating temperature (ambient)	T_{OPR}	0	+65	°C	
Storage Temperature	T_{STG}	– 50	+100	°C	3)
Barometric Pressure (operating & storage)	PBar	+69	+105	kPa	4)
Operating Humidity (relative)	H_{OPR}	10	90	%	
Storage Humidity (without condensation)	H_{STG}	5	95	%	

1) The application designer must meet the case temperature specifications for individual module components.
2) The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR2 DRAM component specification.
3) Storage Temperature is the case surface temperature on the center/top side of the DRAM.
4) Up to 3000 m.

For more information, please contact your AENEON representative